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Design-for-Testability Architectures for 3D Integrated Circuits with Through-Silicon Via Fault Diagnosis: A Comprehensive Review and Future Directions

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Abstract:
Stacking dies with through-silicon vias (TSVs) shortens interconnects and raises bandwidth, but every extra stacking step brings defect mechanisms that planar test flows were never built to catch. One bad TSV can sink a stack of otherwise good dies, so test access, detection and, above all, diagnosis largely decide whether a 3D product makes money. We review peer-reviewed work from about 2010 to 2026, along with a handful of earlier foundational papers, on design for testability (DFT) in TSV-based 3D ICs and on TSV fault diagnosis. The review covers TSV structure, fabrication and electrical behavior, and it proposes a fault taxonomy that separates manufacturing, parametric, environment-induced and lifetime mechanisms. It then compares test-access architectures (including IEEE Std 1838), scan and compression, built-in self-test, contactless pre-bond methods, online testing, redundancy and thermal-aware scheduling. A separate section looks at machine-learning diagnosis: which features, models, datasets and metrics the literature actually uses. What we find is that ML results look promising but rest mostly on simulated or small experimental datasets, and few have been checked against physical failure analysis. We finish with a gap analysis, a roadmap, and specific PhD-level topics on AI-assisted DFT, thermal-aware multi-fault diagnosis, chiplet-level test and repair, reliability-aware diagnosis, digital twins and self-diagnosing stacks.
Keywords:
3D integrated circuits, built-in self-test, design for testability, fault diagnosis, machine learning, test access mechanism, thermal-aware testing, through-silicon vias.

1. INTRODUCTION

The case for vertical integration starts with wires. Cutting a planar chip into blocks on separate strata, joined by short vertical links, shortens interconnect and makes it easier to mix technologies on one system [1]. TSVs turned that idea into something manufacturable. High-density TSVs for 3-D LSIs and the surrounding process technology were reported through the late 2000s [2]–[4], an 8 Gb 3-D DDR3 DRAM showed TSV stacking in memory [5], and cost studies asked what a low-cost TSV technology would demand [6]. The same approach now sits behind 2.5D interposers, TSV-based 3D stacked ICs (3D-SICs), hybrid-bonded stacks and chiplet systems [7], [8].

Testing such parts is harder than testing a monolithic die. Marinissen sorts the difficulties into test flows, test contents and test access [7]: where in manufacturing to test, what new defects to look for, and how to get stimuli to dies that are buried in the stack and unreachable from the pins. The economics make it worse. Once a die is bonded, a faulty TSV can force the known-good dies bonded with it to be thrown away [9], [10].

Pass/fail is not enough either. It cannot say which TSV failed, whether several failed together, or whether a weak defect is going to get worse in the field. Diagnosis gives the location and type of a defect, which is what repair with spare TSVs, yield learning and root-cause analysis need [11]–[13]. We therefore treat detection and diagnosis as related but separate problems, and we pay particular attention to multiple-fault diagnosis, where many published methods stop short.

Contributions. We (i) pull TSV structure, electrical models and fault mechanisms into one taxonomy (Section 3); (ii) compare DFT architectures and test methods on access, coverage, cost and thermal behavior (Section 4); (iii) analyze detection and diagnosis, with an information-theoretic view of multiple-fault localization (Section 5); (iv) review machine-learning diagnosis, including features, datasets and metrics (Section 6); and (v) derive a gap analysis, a roadmap and PhD-level topics (Sections 7 to 9).

Scope and method. This is a narrative critical review, not a PRISMA-style systematic one. We located sources through publisher and index records (IEEE Xplore, Springer, ACM Digital Library, Elsevier and MDPI platforms, Nature Portfolio, dblp and institutional repositories) and favored IEEE, ACM, Springer, Elsevier and other established venues. Coverage runs from about 2010 to September 2026; older papers appear only as foundations. Each reference was checked against a bibliographic record, and where a paper sits behind a paywall we worked from its abstract and metadata. Numbers are quoted only when the cited source states them. Statements that are our own reading of the evidence are marked as assessments.

2. BACKGROUND: 3D INTEGRATION, TSV ARCHITECTURE, AND ELECTRICAL BEHAVIOR

A. Evolution of 3D Integration

Early analysis showed that splitting a planar chip into vertically connected blocks can cut wire-limited area and improve performance, at the price of concentrated power dissipation and harder thermal management [1]. After that the TSV world branched (see Table I). In 2.5D integration, several dies sit side by side on a passive silicon interposer containing TSVs. In a 3D-SIC, active dies are stacked into towers with TSVs between them [7]. Monolithic 3D builds device tiers one after another, has its own diagnosis problems, and has recently drawn learning-based fault localization [14]. Hybrid-bonded stacks with bond pitches below 10 µm have been reported, and chiplet ecosystems are being standardized around die-to-die interfaces such as UCIe [8], [15]. Fig. 1 places the test-related milestones we discuss on one axis.

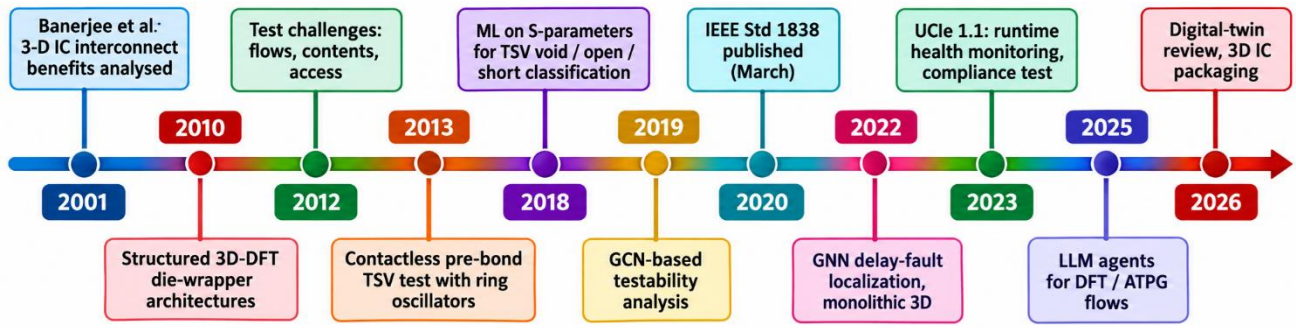


Fig. 1. Selected milestones in 3D-IC test and diagnosis referenced in this review (ordinal spacing, not to scale). Sources: [1], [7], [8], [14]–[21].

Table 1: Integration Styles and Their Main Test Implications

Style	Structure	Test implication	Refs.
2.5D (interposer)	Dies side by side on a passive silicon interposer with TSVs	Interposer interconnect must be tested; active dies are reached through the interposer	[7]

Style	Structure	Test implication	Refs.
TSV-based 3D-SIC	Active dies stacked in towers; TSVs between dies	Pre-, mid- and post-bond test; upper dies are reached through lower dies; wrappers and standardized access needed	[7], [20], [22]
Monolithic 3D	Device tiers built sequentially on one substrate	Fine-grained vertical connections; delay-fault localization across tiers is an active learning-based target	[14]
Hybrid-bonded / chiplet	Fine-pitch bonded interfaces; die-to-die links such as UCIe	Buried interfaces limit in-line observability; interface specifications now include runtime health monitoring and repair	[8], [15]

Assessment: TSV-centric DFT methods are least mature for the last row.

B. TSV Structure and Fabrication

A TSV is a conductor, usually copper or tungsten, running through a thinned silicon substrate and separated from it by a dielectric liner [7]. Processes are usually grouped by when the via is made relative to front-end and back-end processing, and they share a common sequence: etch, liner and barrier deposition, metal fill, planarization, wafer thinning and bonding [2], [23]. The design space is wide. One inspection study uses tungsten-lined open TSVs 100 µm in diameter and 250 µm deep, far bigger than the fine-pitch vias in dense stacks [24]. Each process step maps onto a defect: voids come from electroplated fill, delamination from thermal-expansion mismatch, and cracks from global stress in a warped die [24]. Blind and open-sleeve variants have needed their own pre-bond test circuits [25].

C. Electrical Characteristics

Electrically, a TSV is a short vertical wire with resistance, a capacitance to the substrate and some inductance. Compact models give these as functions of geometry and material and check them against simulation and measurement [26]–[28]. To first order, a cylindrical via of radius r and height h with resistivity ρ has

$$R_{TSV} = \frac{\rho\, h}{\pi\, r^2} \tag{1}$$

and, for a coaxial oxide liner of thickness t_{ox}, a liner capacitance of roughly

$$C_{ox} \approx \frac{2\pi\, \varepsilon_{ox}\, h}{ln\left(\frac{r + t_{ox}}{r}\right)} \tag{2}$$

where ε_{ox} is the liner permittivity. The full models add depletion, frequency dependence and neighbour coupling. Coupling between TSVs, both capacitive and inductive, matters once they are packed densely [28], [29], and a book-length treatment covers signal, power and thermal integrity [30]. The modeling choice follows the test method. High-frequency S-parameter approaches keep the full RLC structure, whereas delay-based methods treat an unbonded TSV as a capacitive load on its driver and look for defect-induced changes in R and C [17].

D. Test Flow Implications

Testing can happen before bonding (pre-bond), on partial stacks (mid-bond), on complete stacks (post-bond), after packaging and at board level. A standardizable die-level wrapper covers all of these and adds low-bandwidth in-field test and debug [22]. Pre-bond TSV test is the tight spot. Before thinning, TSVs are buried and cannot be touched; after thinning they are exposed, but they are small and probing risks damage [17]. That access problem is what pushes designers toward contactless and on-chip methods (Section 4).

3. TSV FAULT MODELS AND TAXONOMY

We organize TSV faults by cause (Fig. 2): manufacturing faults present after fabrication and bonding; parametric faults that degrade timing or noise margin without an outright logic failure; environment-induced faults that depend on temperature and stress; and lifetime faults that appear or grow in the field. Table 2 summarizes the classes.

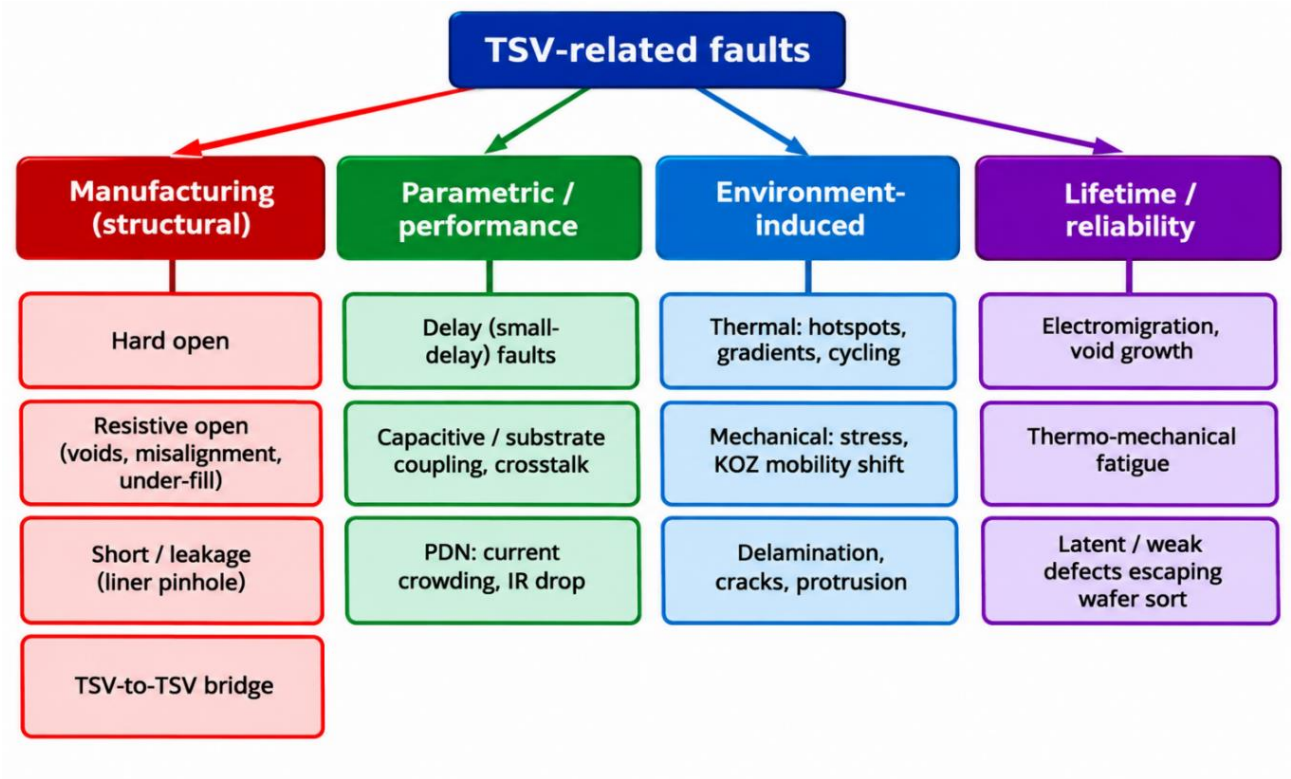


Fig. 2. Proposed taxonomy of TSV-related faults (the mechanisms cited in Section 3).

A. Open and Resistive-Open Faults

Voids, misalignment and incomplete fill can add series resistance or break the conduction path outright. Defect modeling and measurement work shows how such opens change TSV behavior [31], [32], and spare allocation for TSV opens has been posed as an optimization problem [11]. Electrical models of manufacturing faults also underpin multi-tone and ring-oscillator diagnosis: in simulation, a multi-tone dither test separated voids (down to ohm-level resistance) and pinholes (up to megohm level) using a peak-to-average ratio [33], and an earlier fault-modeling and dither scheme appeared in a special issue on 3D-stacked IC test [34]. Resistive opens are awkward because they can pass a logic test and merely shift delay, and because their position along the via changes the signature [35].

B. Short, Leakage, and Bridging Faults

A pinhole in the liner gives the TSV a conduction path to the substrate, which is a leakage fault; dedicated self-test circuits target it [36], and the void and pinhole self-test approaches have been compared head to head [37]. Ring-oscillator methods detect resistive opens and leakage through their effect on delay [17], [35]. Opens and shorts in daisy-chained TSVs have also been located from low-frequency impedance measurements [38], and supervised learning has been applied to void, short and open classification from S-parameters [18]. On the circuit side, one structure detects signal degradation from resistive shorts in the liner oxide and from weak opens or bonding resistance, and reconfigures itself as a signal-recovery circuit for moderate defects [39].

C. Delay and Small-Delay Faults

Delay faults are more common in 3D stacks than in older technologies. Resistive bridges and vias, power droop and crosstalk all contribute, TSV-induced mechanical stress adds to them, and delay-fault

testing is needed for adequate coverage [40]. Because some of these faults depend on temperature gradients, a test run at the wrong thermal state can miss them [40], [41].

D. Coupling, Crosstalk, and Power-Delivery Faults

Full-chip analysis and optimization of TSV-to-TSV coupling has been developed at design level [29], and separate book chapters cover noise coupling and shielding [30]. On the power side, DC current crowding in TSVs affects power integrity [42]. Open defects in power TSVs can be found by measuring resistances between micro-bumps on the power network, but manufacturing variability limits diagnostic performance and motivated a variability-cancellation step; in simulation, both a direct and a middle placement of micro-bumps reached practical diagnostic levels with it [43].

E. Thermal and Mechanical Faults

TSV fabrication leaves tensile stress in the surrounding silicon, which shifts carrier mobility in nearby devices. Keep-out zones limit the effect but cost area, so stress-aware placement and timing analysis try to exploit it instead [44], [45]. Full-chip work has also addressed interfacial cracking [46]. Experiments have examined thermal-stress delamination [47], and in Cu TSV daisy chains, resistance rose with the number of thermal cycles because voids formed and propagated at several interfaces [48]. Cycling can also be used deliberately: a schedule-based technique creates temperature cycling during test to accelerate the protrusion and void formation that cycling causes [49], [50]. Test itself brings thermal risk. Stacking and the high toggle rates of structural patterns produce hotspots that can damage good parts and cost yield [51].

F. Lifetime and Latent Faults

Electromigration and TSV stress make resistive-open and leakage defects worse over time, so a marginal TSV that passes wafer sort may show up, or fail, in the field [17]. Run-time detection of multiple, clustered defects matters for the same reason: low yield and sensitivity to thermal hotspots and stress affect TSV links in service [52].

Table 2: TSV Fault Classes, Mechanisms, and Representative Detection or Diagnosis Approaches

Fault class	**Physical origin**	**Electrical manifestation**	**Detection / diagnosis approaches**	**Refs.**
Hard / resistive open	Voids, misalignment, incomplete fill	Series R; delay or no conduction	Ring oscillators, spare allocation, S-parameter ML, multi-tone dither	[11], [18], [31], [33], [35]
Short / leakage	Liner pinhole; TSV-substrate path	Shunt conductance to substrate	Pinhole self-test, RO with multiple voltage levels, low-frequency impedance	[17], [36]–[38]
Delay (parametric)	Resistive bridges/vias, stress, droop	Timing degradation, temperature-dependent	Delay-fault test at controlled thermal state	[40], [41]
Coupling / PDN	Dense TSV arrays; current crowding	Crosstalk, IR drop	Coupling analysis; PDN resistance measurement	[29], [42], [43]
Thermal	Hotspots, gradients, cycling	Temperature-dependent faults; test-induced damage	Thermal-aware scheduling; temperature-cycling screens	[40], [50], [51]
Mechanical	CTE mismatch, warpage, TSV stress	Mobility shift; delamination, cracks, voids	Stress-aware analysis; failure analysis; acoustic and optical localization	[44], [46]–[48], [53]

Fault class	Physical origin	Electrical manifestation	Detection / diagnosis approaches	Refs.
Lifetime	Electromigration; fatigue	Growing R or leakage	Online monitoring; ECC-based localization	[17], [54]

4. DFT ARCHITECTURES FOR TSV BASED 3D ICS

Fig. 3 lays out the approaches covered in this section, and Table 3 and Table 4 compare them.

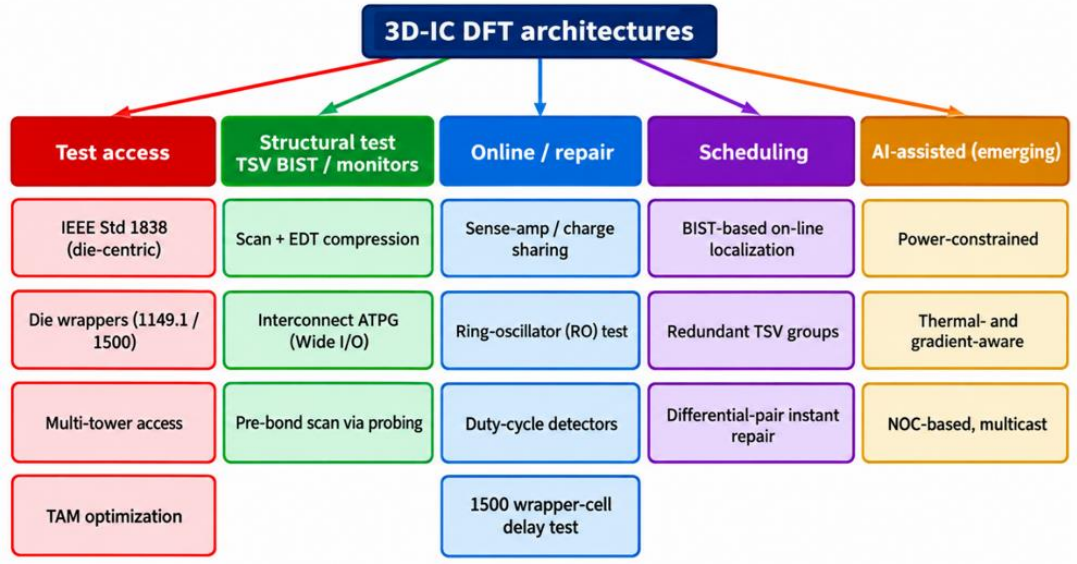


Fig. 3. Taxonomy of DFT approaches for 3D ICs used in this review(the AI-assisted branch is emerging and is examined in Section 6).

A. Test Access Architectures and Standards

Early 3D DfT work proposed structured, scalable test access built on die-level wrappers [16], [55]. The architecture wraps each die so that dies, embedded cores, TSV interconnect and external I/O can be tested as separate units. It supports pre-bond, mid-bond, post-bond and board-level test plus low-bandwidth in-field test and debug, and it exists in variants based on IEEE Std 1149.1 and IEEE Std 1500 [22]. That modularity also yields yield monitoring and first-order fault diagnosis [22]. A generic version handles stacks with any number of towers, sub-towers included [56], and a later tool flow added test data compression, embedded cores and multiple towers [57].

IEEE Std 1838-2019 standardizes this family of architectures. It is die-centric: it defines die-level features that, when compliant dies are stacked, form a stack-level architecture carrying control and data signals for testing intra-die circuitry and inter-die interconnect, before and after stacking, on partial and complete stacks, and at pre-package, post-package and board level. TSVs are the main target, though other interconnect is not excluded [20]. An amendment extends the methodology to external interconnect of multi-die assemblies whose dies carry IEEE 1149.1 boundary-scan register segments [20]. Optimization of test architectures and schedules for TSV stacks builds on this access model [58]–[60].

B. Scan, Compression, and Interconnect ATPG

Embedded deterministic test (EDT) reduces scan test data volume and test time by one to two orders of magnitude in planar designs [61], and 3D tool flows now combine compression with wrappers and multiple towers [57]. Before bonding, scan test of die logic has been demonstrated through TSV probing [62]. For inter-die interconnect, a DfT architecture with ATPG was developed for JEDEC Wide-I/O memory-on-logic stacks [63]; test-sequence derivation for TSV diagnosis is taken up in Section 5 [13].

C. Built-In Self-Test and On-Chip TSV Monitors

On-chip circuits get around the probing problem. Sense-amplification schemes screen TSVs before wafer thinning and bonding using charge sharing [64], and a companion scheme addresses blind and open-sleeve TSVs [25]. A post-bond BIST scheme targets assembled stacks [65], BIST methods have been proposed for pre-bond test [66], and a pre-/post-bond structure with signal recovery characterizes and repairs defect-induced degradation [39]. Oscillation-based methods put the TSV in a ring whose period reflects its RC parameters [17], [67]. To first order, a ring of N inverting stages oscillates with period

$$T_{osc} = 2\,\Sigma_{i=1}^{N} t_{pd,i} \tag{3}$$

where each stage delay follows driver resistance and total load:

$$t_{pd} \approx 0.69\,R_{drv}(C_{TSV} + C_L) \tag{4}$$

A resistive open or a leakage path therefore shifts the measured period (Fig. 4 gives an illustrative curve). Several supply voltages help separate defect types, and the same framework provides contactless pre-bond test and diagnosis [17], [35]. Duty-cycle detectors add a second observable [68]. Other wrapper-based methods reuse IEEE Std 1500 cells and vary TSV driver strength and test clock frequency to expose defects [69].

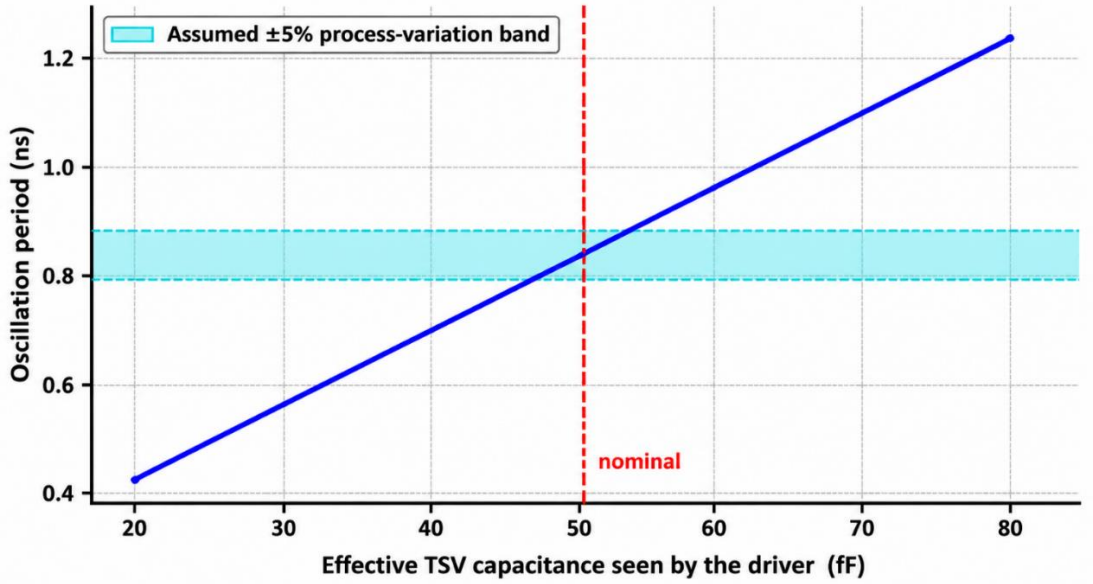


Fig. 4. Illustrative ring-oscillator period versus effective TSV capacitance from Eqs. (3) and (4). Assumed values, not taken from any cited work: N = 5, R_drv = 2 kΩ, C_L = 10 fF, nominal C_TSV = 50 fF, ±5% process-variation band. A defect is detectable only when the shift leaves the band.

D. Pre-Bond Probing and Contactless Access

Where probing is possible, a network of TSVs can be tested together. Session-design algorithms cut test time while still identifying a given number of faulty TSVs uniquely [70], [71], and the idea extends to scan test of die logic [62]. Contactless alternatives avoid probe damage but need calibrated on-die measurement [17], [35]. Wrappers, self-test circuits, probing and scheduling are collected in a book-length treatment [60].

E. Online Testing and In-Field Operation

Online methods test TSVs while the system runs. An online fault-tolerance technique for TSV-based 3-D ICs has been proposed [72]. TSV-OCT detects opens and shorts in parallel with data transactions using error-correcting codes, then localizes them; in Monte Carlo simulation its statistical detector finds twice as many faults as conventional ECC-based techniques, isolation-and-check localizes up to four to five times more defects, and response time stays under 65,000 cycles [54]. A related non-

blocking method targets multiple defects in 3D network-on-chip links [52], and configurable fault-tolerant serial links protect inter-die communication [73]. The UCIe 1.1 specification added runtime health monitoring and repair for high-reliability use, plus compliance-test enhancements [15].

F. Redundancy, Repair, and Hybrid Architectures

Redundant TSVs turn diagnosis into yield. Under one probabilistic model, three or more failed TSVs in a tier occur with probability below 0.002%, so provisioning for two failures covers 99.998% of cases; with one redundant TSV per block, blocks of at most 50 or 25 TSVs give 90% or 95% recovery for two failures [9]. The journal version generalizes the architecture and design issues [74]. Later work covers effective repair [12], cost-effective TSV grouping [75] and ring-based redundancy for clustered faults [76]. Differential signaling uses two TSVs per binary signal, giving instant test and repair with no global result analysis or complex reconfiguration, which suits multi-vendor stacks where die providers cannot support elaborate schemes [10]. The clustered-fault work is a warning that the independence assumption behind small redundancy budgets can fail [52], [76]. Fig. 5 collects the quantitative results quoted in this section and in Section 6.

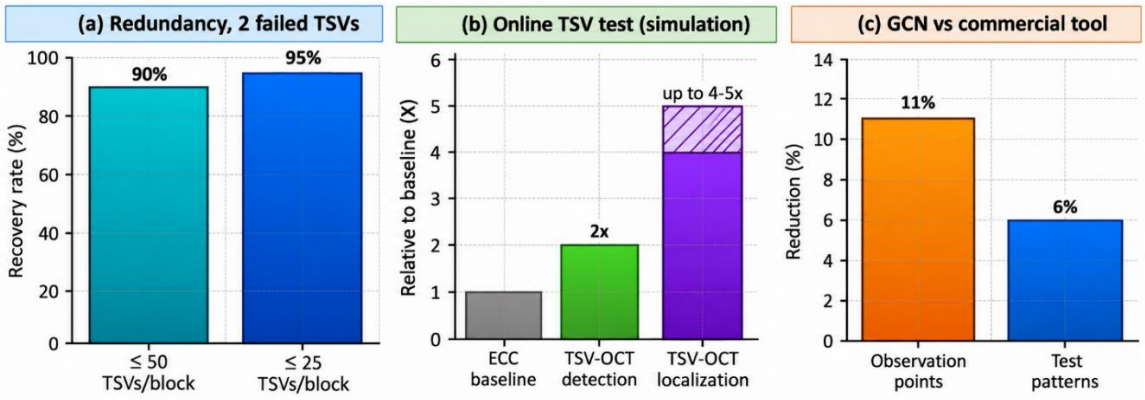


Fig. 5. Quantitative results as reported by the cited sources. (a) Recovery rate under a probabilistic model [9]. (b) TSV-OCT relative to conventional ECC-based techniques in Monte Carlo simulation [54]. (c) Graph convolutional network for observation-point insertion versus a commercial testability tool at similar coverage [19]. Panels use different metrics and are not comparable with one another.

G. Power- and Thermal-Aware Test Scheduling

Scheduling decides how much of the TAM and power budget a test consumes. Power-constrained scheduling for core-based 3D stacks co-optimizes wafer sort and package test [77]. Thermal awareness adds two ideas. First, faults that depend on temperature gradients need the right thermal state, which can be produced by applying heating sequences through the TAM instead of an external heater, guided by thermal simulation [40]; the approach was extended to burn-in and delay-fault test [41]. Second, test must not itself create damaging hotspots, which is what multicast and thermal-aware scheduling address for stacked network-on-chip test access [51]. A first-order thermal model for die k in a stack is

$$T_k = T_{amb} + \Sigma_m R_{km} P_m \quad (5)$$

with ambient temperature T_{amb}, thermal-resistance coupling R_{km} between blocks k and m, and block power P_m. Upper dies shed heat mostly through the dies below them, so the coupling terms make peak temperature a property of the whole stack rather than of one die. Fig. 6 shows the effect with assumed numbers (assessment).

Table 3: Comparison Of DFT Architectures and Test-Access Approaches

Approach	Scope	Key mechanism	Assessment of gaps	Refs.
IEEE Std 1838	Die-centric access for intra-die and	Standard die-level features forming a	Defines access, not diagnostic data	[20]

Approach	Scope	Key mechanism	Assessment of gaps	Refs.
	inter-die test, pre- to post-stack	stack-level test access architecture	formats or ML interfaces	
Die wrapper (1149.1 / 1500 variants)	Pre-, mid-, post-bond, board, in-field	Wrapper per die; modular test of dies, cores, TSVs, I/O	Diagnosis is first-order (unit-level), not TSV-level	[22]
Multi-tower access	Stacks with several towers and sub-towers	Generic architecture for any number of towers	Fine-pitch and hybrid-bond interfaces not treated	[56]
3D DfT with compression and tool flow	Embedded cores, TDC, multiple towers	Automated insertion and pattern generation flow	Thermal effects of compressed patterns not the focus	[57]
Interconnect ATPG (Wide I/O)	Memory-on-logic die stacks	DfT plus ATPG for inter-die tests	Tied to a specific interface	[63]
TAM optimization and scheduling	Test time under TAM and TSV limits	Architecture and schedule optimization	Mostly test time; diagnosis cost rarely modeled	[58], [59]
Power-constrained scheduling	Core-based 3D-SIC	Co-optimized wafer sort and package test	No explicit thermal gradients	[77]
Thermal-aware scheduling	Gradient-dependent faults; NoC-based test	Heating via TAM; hotspot-limited schedules	Not coupled to TSV-level diagnosis	[40], [41], [51]

The "assessment of gaps" column reflects our reading of the cited abstracts and papers.

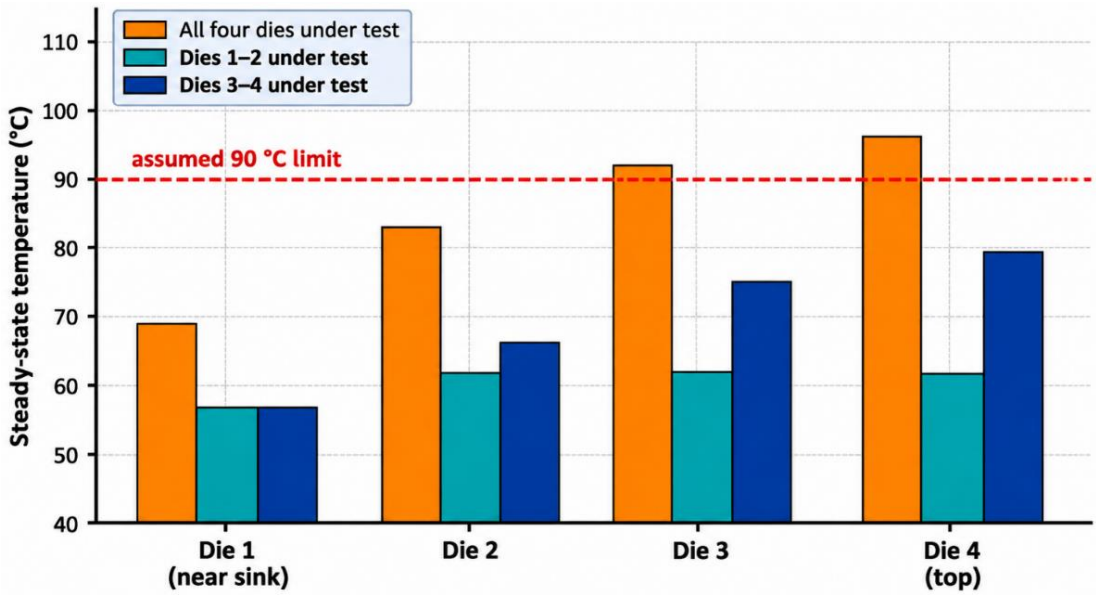


Fig. 6. Illustrative steady-state temperatures for a four-die stack from Eq. (5). Assumed values, not from any cited work: T_{amb} = 45 °C, sink resistance 0.4 K/W, 0.3 K/W per intervening die, 15 W per die under test. Testing all dies at once pushes the upper dies over the assumed limit; testing two at a time does not.

Table 4: Pre-Bond and Post-Bond TSV Test and Diagnosis Methods

Method	Access	Detects	Diagnosis / notable evidence	Stage	Refs.
Sense amplification, charge sharing	On-chip	Pre-bond TSV defects	Screens before thinning and bonding; companion scheme for blind and open-sleeve TSVs	Pre-bond	[25], [64]
Ring oscillators, multiple voltage levels	On-chip, contactless	Resistive opens, leakage	Test and diagnosis via oscillation period; duty-cycle detectors add observables	Pre-bond	[17], [35], [68]
Oscillation-based test	On-chip	TSV defects	Oscillation-based pre-bond TSV test (see Section 4.C)	Pre-bond	[67]
Probing of TSV networks	Probe pads	Faulty TSVs; die logic	Session design identifies a given number of faulty TSVs; ILP-based session optimization; scan test of die logic	Pre-bond	[62], [70], [71], [78]
IEEE 1500 wrapper-cell delay test	Wrapper cells	Delay-type TSV defects	Vary driver strength and test clock frequency	Pre-bond	[69]
Test and signal-recovery structure	On-chip	Liner shorts, weak opens, bonding resistance	Detects degradation; reconfigures as recovery circuit for moderate defects	Pre- and post-bond	[39]
Post-bond BIST	On-chip	TSV defects in stacks	Built-in scheme for assembled stacks	Post-bond	[65]
Test-sequence diagnosis	Interconnect test	Single and multiple defective TSVs	Procedure for diagnosis sequences; pseudorandom patterns evaluated	Post-bond	[13]
Impedance-based location	Measurement	Open and short in daisy chains	Locates defect from low-frequency L and C extraction	Post-bond / lab	[38]
ECC-based online localization	Functional traffic	Open and short, multiple TSVs	Detects 2x more faults than conventional ECC; localizes up to 4x to 5x more; <65,000 cycles	Online	[54]
Differential-pair instant repair	Functional	Faulty TSV in a pair	No global result analysis needed	Online	[10]

5. TSV FAULT DETECTION AND DIAGNOSIS

A. Problem Formulation

Detection asks whether any TSV in a group is faulty, and localization asks which one. Multiple-fault diagnosis wants the full set when d of n TSVs may be defective. Pre-bond probing methods and post-bond interconnect tests all answer some version of that question with a bounded number of measurements [13], [70]. If each test session returns one binary outcome, counting alone bounds how many sessions S are needed to pin down exactly which d of n TSVs are faulty:

$$S \geq \lceil log_2 C(n,d) \rceil \quad (6)$$

because S binary outcomes can tell apart at most 2^S fault sets. We derived the bound ourselves, and it holds only for binary outcomes. Analog measurements such as oscillation period or duty cycle carry more than one bit per session, which is one reason RO-based diagnosis is attractive [35], [68]. Fig. 7 shows how quickly the requirement grows with d: candidate sets multiply combinatorially, so multiple-fault diagnosis is expensive even before noise enters.

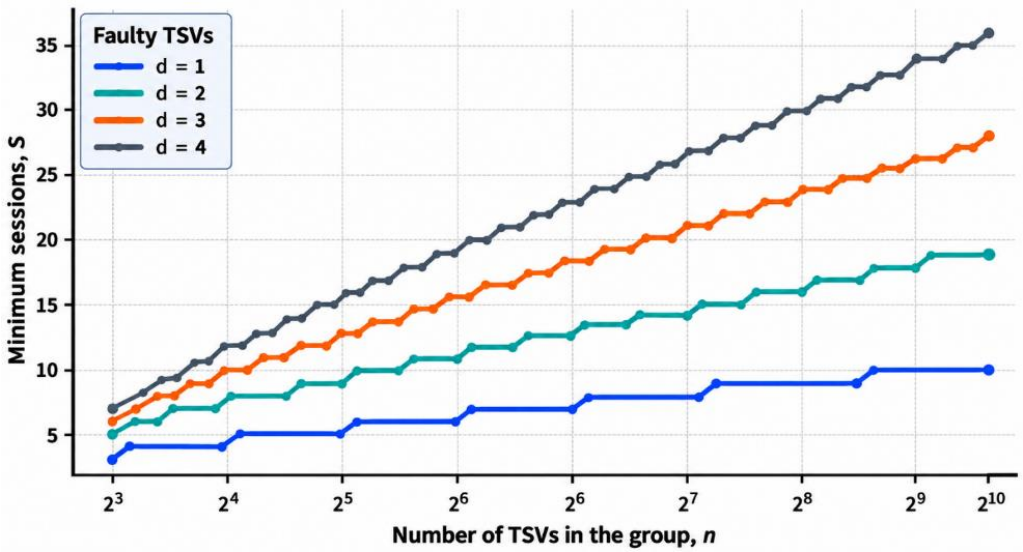


Fig. 7. Lower bound on the number of binary-outcome test sessions needed to identify exactly d faulty TSVs among n, from Eq. (6). Computed values; the bound is our derivation.

B. Localization Techniques

For a probed network of TSVs, an efficient algorithm for parallel test sessions reduces test time while still identifying a given number of faulty TSVs uniquely [70], and a later three-stage method uses integer linear programming, greedy sequencing and early termination to cut test time further without losing that capability [78]. Test-sequence diagnosis takes another route: a procedure derives sequences for single and multiple defective TSVs, and pseudorandom-pattern experiments indicate feasibility and robustness [13]. Contactless RO methods with several voltage levels detect and diagnose resistive opens and leakage [35], and duty-cycle detectors add observables [68]. TSV-OCT localizes multiple defects during operation without halting data transactions [54]. Low-frequency L and C extraction locates opens and shorts in daisy chains [38], and resistance measurement between micro-bumps detects power-TSV opens [43].

Physical failure analysis supplies the ground truth against which any electrical diagnosis should be judged. Lock-in thermography and photoemission microscopy localize electrical shorts in the TSV liner, and gigahertz acoustic microscopy inspects fill defects [79]. Optical beam-based methods localize opens and shorts in micrometer-scale TSV interconnects [53], and lateral emission microscopy has been used to investigate TSV defects [80].

C. Multiple and Clustered Faults

Redundancy budgets are often sized on an independence assumption: under one model, three or more failed TSVs in a tier are so rare that provisioning for two is enough [9]. Clustered defects break that assumption. Ring-based redundancy was proposed specifically for clustered faults [76], and online-

test work stresses detecting multiple, clustered defects [52]. In our reading, a single-fault classifier trained on isolated defects can be misled when neighboring TSVs fail together (assessment). Multi-fault diagnosis under realistic spatial correlation is one of the central open problems (Section 7).

D. Evaluation Dimensions

Accuracy alone will not compare diagnosis methods fairly. Coverage and localization granularity define what can be found, test time and session count define cost [70], power and thermal effects limit how hard a test can be pushed [40], [51], BIST and wrapper area limit adoption [22], and scalability decides whether a method survives dense TSV arrays. Table 5 sets these dimensions against representative approaches. Entries state what the cited sources report; "not reported" means the abstract or reviewed text did not address the dimension.

Table 5: Diagnosis Approaches Against Evaluation Dimensions

Approach	Localization	Multi-fault	Cost evidence reported	Thermal / power treatment	Refs.
Probing-network sessions	Individual TSV	Given number of faults	Test-time reduction via parallel sessions; ILP-based optimization	Not reported	[70], [78]
Test-sequence diagnosis	Individual TSV	Single and multiple	Pseudorandom patterns evaluated	Not reported	[13]
RO + multiple voltages	Test and diagnosis (per title)	Not reported	On-chip circuitry, contactless	Not reported	[35]
Duty-cycle + RO	Test and diagnosis	Not reported	Duty-cycle detectors added to RO structure	Not reported	[68]
Duty-cycle + RO	Test and diagnosis	Not reported	Duty-cycle detectors added to RO structure	Not reported	[68]
ECC-based online (TSV-OCT)	Individual defects	Multiple, clustered	<65,000-cycle response; no performance degradation in a 3D NoC router	Motivated by thermal hotspots and stress	[52], [54]
Differential instant repair	Implicit (pair-level)	Not reported	Two TSVs per binary signal	Not reported	[10]
Thermal-aware scheduling	Not a diagnosis method	n/a	Test-time savings reported for gradient-based scheduling	Explicit thermal control	[40], [51]
Physical failure analysis	3D localization of defects	Not reported	High-resolution imaging is throughput-limited [24]	n/a	[53], [79]

Assessment: no method in this table jointly optimizes multi-fault diagnosis, thermal state and test time.

6. AI AND MACHINE-LEARNING-BASED TSV FAULT DIAGNOSIS

A. Data Modalities and Features

Published TSV diagnosis studies fall into four groups by input. Electrical-response features come from the TSV channel (S-parameters, group delay [18]) or from ring-oscillator structures (oscillation period and duty cycle [81]). Sensor features come from a built-in temperature-sensor array whose readings depend on internal defects [82]. Image features come from X-ray tomography of microbumps [83] and from scanning acoustic microscopy (SAM) C-scans of TSV arrays [24]. Graph features come from netlists and design graphs used for testability and fault localization [14], [19]. The modality decides

where a model can run. Electrical and sensor features are candidates for on-die or ATE deployment; image features suit offline failure analysis and inline inspection.

B. Algorithms and Reported Results

Huang et al. train a supervised classifier on S-parameter data sets of defective and normal TSVs to detect voids, shorts and opens without destroying the part [18]. A later study describes this line of work as semi-automated: models such as k-nearest neighbors and random forests rely on hand-picked features taken from high-frequency structural simulator (HFSS) data for TSVs with and without voids [24]. For ring-oscillator data, Shang et al. use oscillation period and duty cycle as features, a least-squares support vector machine (LSSVM) as the classifier, and particle swarm optimization to tune it. A variant whose inertia weight changes dynamically (W-PSO) diagnosed multi-faults, combining resistive opens and leakage, more accurately than plain PSO-LSSVM [81]. Liu et al. detect defects in a TSV transmission channel with a machine-learning approach [84].

Nie et al. take a thermal route. A built-in temperature-sensor array is laid out so that its readings relate to internal defects such as gaps, bottom voids and missing fill; in simulation, a supervised classifier reaches an accuracy of up to 95.625%, and experiments were used to check the sensor arrangement [82]. Image-based work reports strong numbers under specific conditions. A CNN on 3D X-ray tomography of microbumps predicts operational faults of solder joints with accuracy up to 89.9% [83]. An end-to-end CNN on SAM C-scans localizes TSVs with 100% accuracy and classifies them with more than 96%, on open tungsten-lined TSVs 100 µm in diameter and 250 µm deep, and beats MLP, decision-tree and random-forest baselines that stayed below 90% [24]. That study used wafers with deliberately induced defects, reports training and validation accuracy, and ran the baseline comparison on a 96-image test set [24]. The results fit their purpose, but they should not be read as field diagnostic accuracy (Fig. 8).

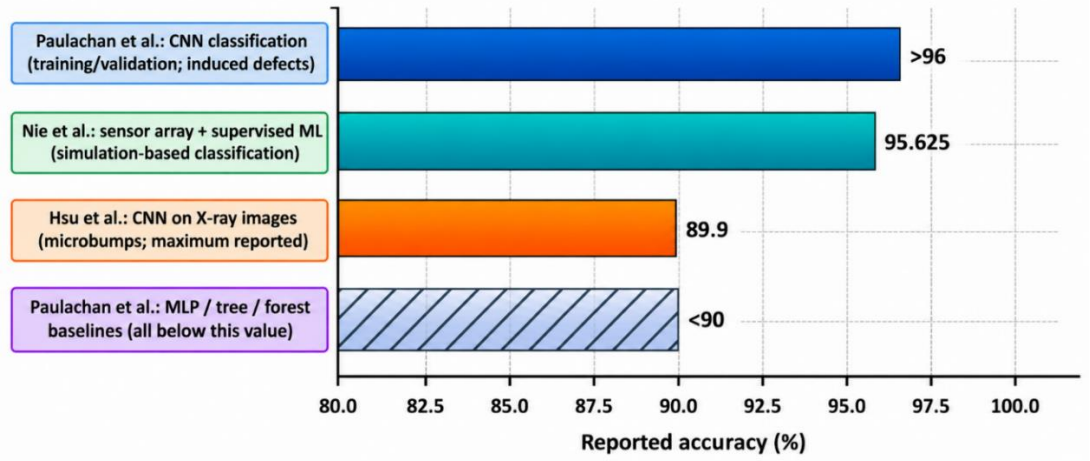


Fig. 8. Accuracies reported by three studies [24], [82], [83]. The tasks, data and evaluation protocols differ (simulation versus imaging, induced versus natural defects, training/validation versus test), so the bars illustrate what has been reported and should not be ranked against each other. The hatched bar is an upper bound ("below 90%").

Graph learning is earlier-stage for TSV-specific tasks. A graph convolutional network for testability analysis predicts hard-to-observe nodes and, inside an observation-point insertion flow, matches a commercial tool's fault coverage with 11% fewer observation points and 6% fewer test patterns [19]. GNN-based delay-fault localization has been built for monolithic 3D ICs [14], and graph convolutional networks have assessed fault criticality in AI accelerators [85]. Reinforcement learning and neural networks have been applied to test point insertion [86], [87]. These are DFT-level methods rather than TSV-level ones, but they offer architectures that a TSV-aware graph could reuse (assessment).

Large language models enter DFT at the workflow level. DFTAgent lets an LLM orchestrate a DFT toolchain and completes the ATPG task cycle on ISCAS'85, ISCAS'89 and ITC'99 benchmarks with fault coverage comparable to a manually scripted baseline [21]. VeriRAG uses retrieval-augmented generation to repair RTL for DFT compliance and calls itself the first LLM-assisted DFT-EDA framework [88]. A recent overview places these trends within the future of DFT and silicon lifecycle

management [89]. For thermal modeling in 3D ICs, operator learning (DeepOHeat) predicts temperature fields 1000x to 300,000x faster than a commercial solver on unseen cases [90], which matters because test scheduling needs thermal estimates much faster than finite-element runs can give.

Table 6: AI/ML Studies Relevant to TSV and 3D-Interconnect Diagnosis

Study	Task	Features	Algorithm	Data source	Reported result	Refs.
Huang et al.	Detect and classify void, short, open in TSVs	S-parameters	Supervised ML classifier	Simulation-derived defect and normal TSV sets	Not quantified in reviewed text	[18], [24]
Shang et al.	Multi-fault (resistive open + leakage) diagnosis	RO period, duty cycle	LSSVM tuned by PSO / W-PSO	Ring-oscillator test structure	W-PSO-LSSVM more accurate than PSO-LSSVM	[81]
Liu et al.	Open and short failures in TSV channel	Not visible in reviewed text	ML approach (per title)	Not visible in reviewed text	Not visible in reviewed text	[24], [84]
Nie et al.	Internal TSV defect classification (gaps, bottom voids, missing fill)	Built-in temperature-sensor array readings	Supervised ML	Simulation, with experiments on the sensor arrangement	Accuracy up to 95.625%	[82]
Hsu et al.	Microbump fault prediction	3D X-ray tomography images	CNN	Collected image database	Accuracy up to 89.9%	[83]
Paulachan et al.	TSV localization and classification	SAM C-scan images	Two-stage end-to-end CNN	Wafers with induced defects, ~10,000 TSVs in ROI	100% localization; >96% classification	[24]
Ma et al.	Observation-point insertion (testability)	Netlist graph	GCN	Netlists compared with a commercial tool	11% fewer OPs, 6% fewer patterns at similar coverage	[19]
Hung et al.	Delay-fault localization, monolithic 3D	Circuit graph	GNN	Monolithic 3D ICs (per title)	Not quantified in reviewed text	[14]

"Not quantified in reviewed text" means the figures were not visible in the sources accessed for this review.

C. Datasets and Evaluation Metrics

Across these studies the data come from three places: electromagnetic or circuit simulation of injected defects [18], [24], [82], test-structure data [81], and wafers with deliberately altered processes imaged by SAM or X-ray [24], [83]. We did not find a publicly released, community-standard benchmark for TSV fault diagnosis; each group builds its own data. The wider packaging-reliability community has called for standardized open datasets for the same reason [8].

Metrics should follow the cost of errors. Accuracy is common, but at production defect rates a classifier that calls everything good can look accurate. Precision, recall and their harmonic mean F1 say more:

$$P = \frac{TP}{TP + FP}, \quad R = \frac{TP}{TP + FN} \tag{7}$$

$$F_1 = \frac{2PR}{P + R} \tag{8}$$

where TP, FP and FN count true positives, false positives and false negatives. Diagnosis adds its own measures: localization error (the share of faults assigned to the wrong TSV), diagnostic resolution (candidate-set size), false-positive rate (a false positive wastes a good TSV and, with redundancy, a spare), calibration of confidence scores, and inference latency and memory for on-die use. We would also hold out whole wafers or dies when splitting data, not random TSVs, to avoid leakage between correlated samples (recommendation).

D. Advantages and Limitations

On the plus side, ML can learn diagnostic signatures from noisy, high-dimensional measurements where fixed thresholds are brittle, it can combine several observables such as period and duty cycle [81], it removes manual image inspection at scale [24], and graph models can generalize across netlists [19].

The limits are just as clear. Simulation-derived training sets risk a simulation-to-silicon gap [18], [24], and deliberately induced defects may not look like natural ones [24]. Test sets can be small [24], and labels for buried defects need destructive analysis, the same data-scarcity problem digital-twin work runs into [8]. Most studies classify isolated defects rather than clustered ones (Section 5.C). Black-box predictors are hard to trust in safety-critical settings [8]. And only electrical and sensor methods fit naturally on a die or an ATE; image-based methods stay offline (assessment).

7. CRITICAL ANALYSIS: LIMITATIONS AND RESEARCH GAPS

Test access and pre-bond electrical test are well covered in the literature. Diagnosis at scale, thermal coupling and lifetime behavior are not. Table 7 lists the gaps, the evidence for each, and the opening each one leaves. Entries marked "assessment" are inferences from the pattern of the surveyed work, not claims by the cited authors.

Table 7: Research-Gap Analysis

#	Gap	Evidence	Consequence	Opportunity
G1	No open benchmark for TSV diagnosis	Each study builds its own data [18], [24], [81]; a call for open packaging-reliability datasets [8]	Results not comparable; hard to reproduce	Community dataset with defect ground truth
G2	Simulation-to-silicon gap	Training on HFSS-derived data [24]; deliberately induced defects [24]; simulation-based sensor classification [82]	Optimistic accuracy; poor transfer (assessment)	Domain adaptation with measured test chips
G3	Clustered and multiple faults	Independence assumption in redundancy sizing [9] versus clustered faults [52], [76]	Single-fault models fail on correlated defects (assessment)	Spatially aware multi-fault diagnosis
G4	Thermal state in diagnosis	Gradient-dependent delay faults [40], [41]; test hotspots [51]	Diagnosis at the wrong temperature can misclassify (assessment)	Temperature-conditioned models and joint scheduling
G5	Fine-pitch and hybrid-bond interfaces	Sub-10 µm bond pitches in industrial stacks [8]	TSV-centric methods may not transfer (assessment)	Diagnosis for bond interfaces and chiplet links
G6	Latent defects and aging	Opens and leakage worsen over time [17]; resistance rises with thermal cycling [48]; run-to-failure data scarce [8]	Escapes at wafer sort; limited prognostics	Aging-aware diagnosis with physics priors

#	Gap	Evidence	Consequence	Opportunity
G7	Standards for diagnostic data	IEEE 1838 defines access [20]; UCIe adds health monitoring and repair [15]; standards-aligned roadmap proposed [8]	No common format for diagnostic results or model updates (assessment)	Diagnostic data records over 1838 / UCIe
G8	Explainability and trust	Black-box limits trust [8]	Slow industrial adoption	Physics-constrained, explainable models
G9	AI-for-DFT maturity	LLM DFT agents evaluated on academic benchmarks [21]; RTL repair still early [88]	Unproven at 3D-stack scale	3D-aware, verified agent flows

8. FUTURE DIRECTIONS AND RESEARCH ROADMAP

A. AI-Assisted DFT

AI help already shows up at three levels. At design level, LLM agents and retrieval-augmented generation automate DFT scripting and RTL testability repair [21], [88]. At algorithm level, graph models and reinforcement learning improve test point insertion and fault localization [14], [19], [86]. At data level, ML classifies TSV defects from electrical, sensor and image data (Section 6). What is missing is a connection between the three around the IEEE 1838 model: an agent that inserts and verifies 1838-compliant wrappers, a GNN that localizes faults over stack-aware netlists, and a classifier that consumes on-die monitor data. Verification loops are essential, because a wrong wrapper or schedule can quietly reduce coverage.

B. Thermal-Aware Testing and Diagnosis

Temperature changes both what a test finds and what it damages [40], [51]. Future work should treat temperature as an input to the diagnostic model and not only as a constraint on the schedule. Fast surrogates such as operator-learning thermal predictors make real-time thermal estimates during test plausible [90], and Eq. (5) suggests that stack-level coupling, not per-die power, sets the limit. A joint formulation would pick test sessions to maximize diagnostic information per unit of thermal budget.

C. Chiplet and 3D Integration

IEEE 1838 gives die-level access for TSV stacks [20], while chiplet interfaces such as UCIe add runtime health monitoring, repair and compliance-test features [15]. Bridging the two matters for heterogeneous stacks that mix TSV, micro-bump and hybrid-bond links. The agenda includes shared diagnostic hooks for TSV and die-to-die lanes, repair policies that span link types, and known-good-die strategies for multi-vendor assemblies, which the differential-pair scheme already targets for TSVs [10].

D. Reliability-Aware Diagnosis

A defect that passes wafer sort may worsen through electromigration and stress [17], and thermal cycling raises TSV resistance through void formation [48]. Diagnosis should therefore output a risk estimate as well as a class label: how likely is this TSV to fail within the mission profile? Physics-of-failure priors can regularize learning when run-to-failure data are scarce [8], and cycling-based test schedules can act as a screen [50].

E. Digital Twins

A recent critical review separates digital models (offline simulation), digital shadows (one-way monitoring) and digital twins (closed-loop feedback), and finds that most reported "twins" for 3D IC packaging are really models or shadows [8]. For test, a twin could take in wafer-sort, RO and thermal data, update a hybrid physics-ML model, and adapt test limits and sessions. The same review names latency, data sparsity and observability as the barriers [8], which line up with the gaps in Table VII.

F. Self-Diagnosing Architectures

Fig. 9 sketches a self-diagnosing 3D-IC architecture that pulls these directions together. On each die or chiplet, monitors (RO and duty-cycle structures, thermal and stress sensors, link error counters) feed

a small classifier through the standard test access path. The classifier drives repair by spare-TSV steering and mitigates test-time thermal risk. An off-stack hybrid twin receives compressed features, refines models and thresholds, and sends updates back. The design is our proposal, not a reported implementation; ECC-based online localization [54] and differential repair [10] are the closest published building blocks.

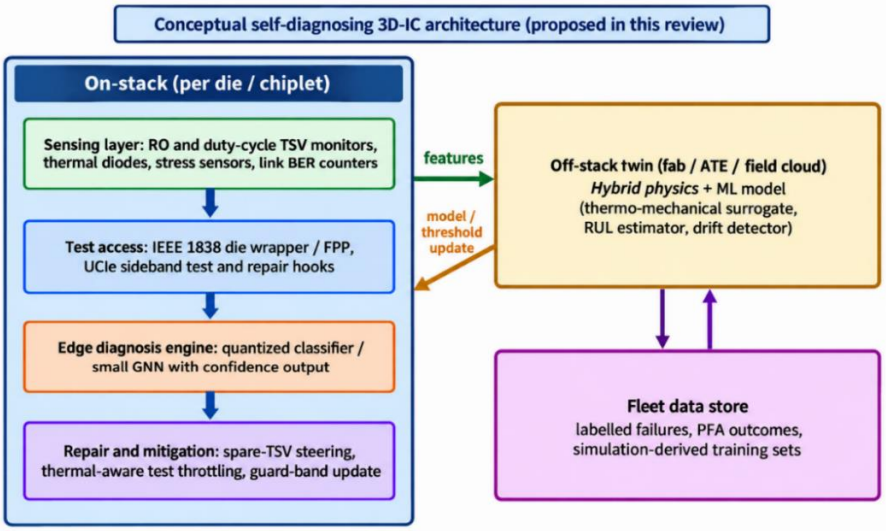


Fig. 9. Conceptual self-diagnosing 3D-IC architecture proposed in this review. On-stack sensing, test access, edge diagnosis and repair are coupled to an off-stack hybrid physics-ML twin that supplies model and threshold updates.

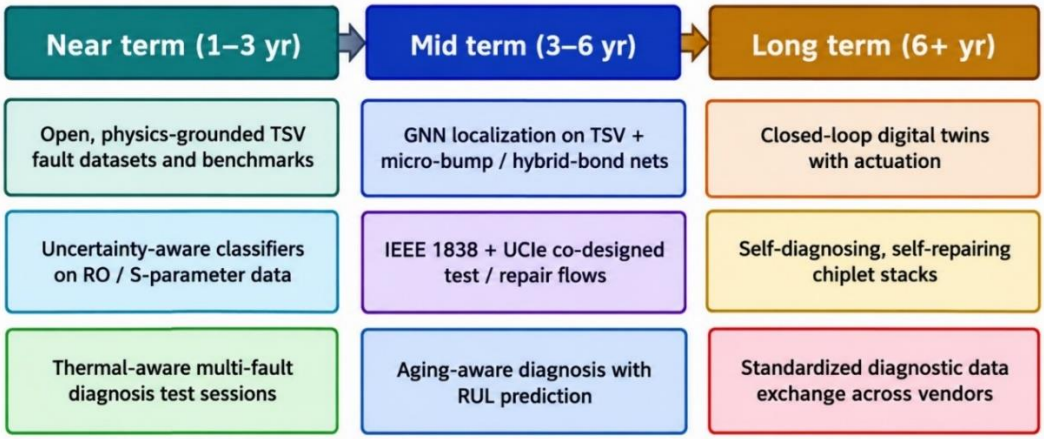


Fig. 10. Research roadmap by horizon (our proposal, derived from the gaps in Table VII).

9. RESEARCH GAPS AND POTENTIAL TOPICS FOR RESEARCH

Each topic below gives a research question, an approach and a way to judge success. First steps can use the published building blocks cited in this review.

1. **Open, physics-grounded TSV diagnosis benchmark (G1, G2).** *Question:* can a dataset that combines calibrated multiphysics simulation with silicon test-chip measurements support reproducible comparison of diagnosis methods? *Approach:* inject opens, leakage and bridges with process variation, measure RO period, duty cycle and S-parameters on test chips, and release splits by wafer and die. *Evaluation:* simulation-to-silicon transfer loss, precision and recall, localization error.
2. **Uncertainty-aware multi-fault diagnosis with clustered priors (G3).** *Question:* how far can diagnosis go when faults are spatially correlated? *Approach:* Bayesian or conformal classifiers with adaptive session design in the spirit of probing-network sessions [70], [78]. *Evaluation:* sessions needed against the bound of Eq. (6), and calibration under clustering.
3. **Thermal-conditioned joint diagnosis and scheduling (G4).** *Question:* can temperature-aware diagnostic models plus thermal surrogates raise diagnostic information per unit of thermal

budget? *Approach:* combine gradient-aware scheduling [40], [41] with operator-learning thermal prediction [90]. *Evaluation:* diagnostic resolution, test time, thermal-limit violations.

4. **GNN fault localization across TSV, micro-bump and bond nets (G5).** *Question:* can graph models trained on monolithic-3D delay faults [14] extend to TSV-based stacks with coupling and thermal edges? *Approach:* graphs with physical adjacency and power-map features. *Evaluation:* localization accuracy and inference cost on 3D benchmark circuits.
5. **IEEE 1838 and UCIe co-designed test, diagnosis and repair (G7).** *Question:* what minimal diagnostic data record and access hooks let one flow serve TSV and die-to-die lanes? *Approach:* extend the 1838 access model [20] with UCIe sideband health and repair features [15]. *Evaluation:* area, test time and interoperability across mixed stacks.
6. **Reliability-aware TSV diagnosis with remaining-life estimates (G6).** *Question:* can weak-defect signatures predict field failure? *Approach:* fuse RO and sensor monitors with electromigration and thermal-cycling priors [48] and use accelerated tests and transfer learning to offset scarce run-to-failure data [8]. *Evaluation:* time-to-failure prediction error and screening escape rate.
7. **Hybrid physics-ML digital twin for test-flow adaptation (G6, G8).** *Question:* does closing the loop, from measured test data to updated limits and sessions, reduce escapes without overkill? *Approach:* physics core plus ML surrogate with data assimilation [8]. *Evaluation:* escape rate, yield loss, twin fidelity, update latency.
8. **Self-diagnosing, self-repairing stack (Fig. 9).** *Question:* what are the hardware cost and latency of on-die classification plus spare-TSV steering? *Approach:* quantized classifier on monitor data, compared with ECC-based online localization [54] and differential repair [10]. *Evaluation:* area, power, diagnosis latency, repair coverage.
9. **Verified LLM agents for 3D DFT (G9).** *Question:* can agents generate and verify 1838-style wrapper insertion and schedule optimization with formal or simulation checks? *Approach:* extend orchestration and retrieval frameworks [21], [88] to stack-level constraints. *Evaluation:* coverage parity with expert scripts, error-recovery rate, verification cost.
10. **Explainable diagnosis (G8).** *Question:* can predictions be tied to physical parameters such as the R and C of Eqs. (1) to (4)? *Approach:* physics-constrained features and attribution validated by failure analysis [53], [79]. *Evaluation:* agreement between attributions and physical failure analysis.

Validation resources matter as much as algorithms. Topics 1, 6 and 10 need test chips and failure-analysis access (thermography, acoustic or optical localization) to provide ground truth [53], [79].

10. CONCLUSION

TSV-based 3D ICs have a mature test-access story, anchored by die wrappers and IEEE Std 1838, and a growing set of pre-bond, post-bond and online TSV test methods. Diagnosis is less mature. Single defects are well studied. Multiple and clustered defects, temperature-dependent behavior and lifetime drift are not. Machine learning has produced encouraging results on S-parameter, ring-oscillator, sensor and image data, but the evidence rests on simulated or small experimental datasets without a common benchmark, and few studies validate against physical failure analysis. The most useful next steps are open datasets, uncertainty-aware multi-fault models, thermal-conditioned diagnosis, integration with IEEE 1838 and chiplet-interface features, and closed-loop digital twins.

Limitations of this review. The survey is selective, not exhaustive. For paywalled works we relied on abstracts and metadata, and some contemporaneous work may be missing. The illustrative figures (RO period and stack temperature) use assumed parameters and are not results from any cited paper. Assessments and proposals are ours and are labeled as such.

DECLARATIONS:

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Data Availability Statement : The data presented in this study are available upon request from the corresponding author.
Use of Generative Artificial Intelligence : AI-assisted tools have been used to improve language editing or grammatical clarity, the authors take full responsibility for the content of the final version.

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